

REMARKS

Claims 1-9 have been rejected under 35 U.S.C. § 112 for an informality. The specification has also been objected to for lack of sufficient description in the drawings section.

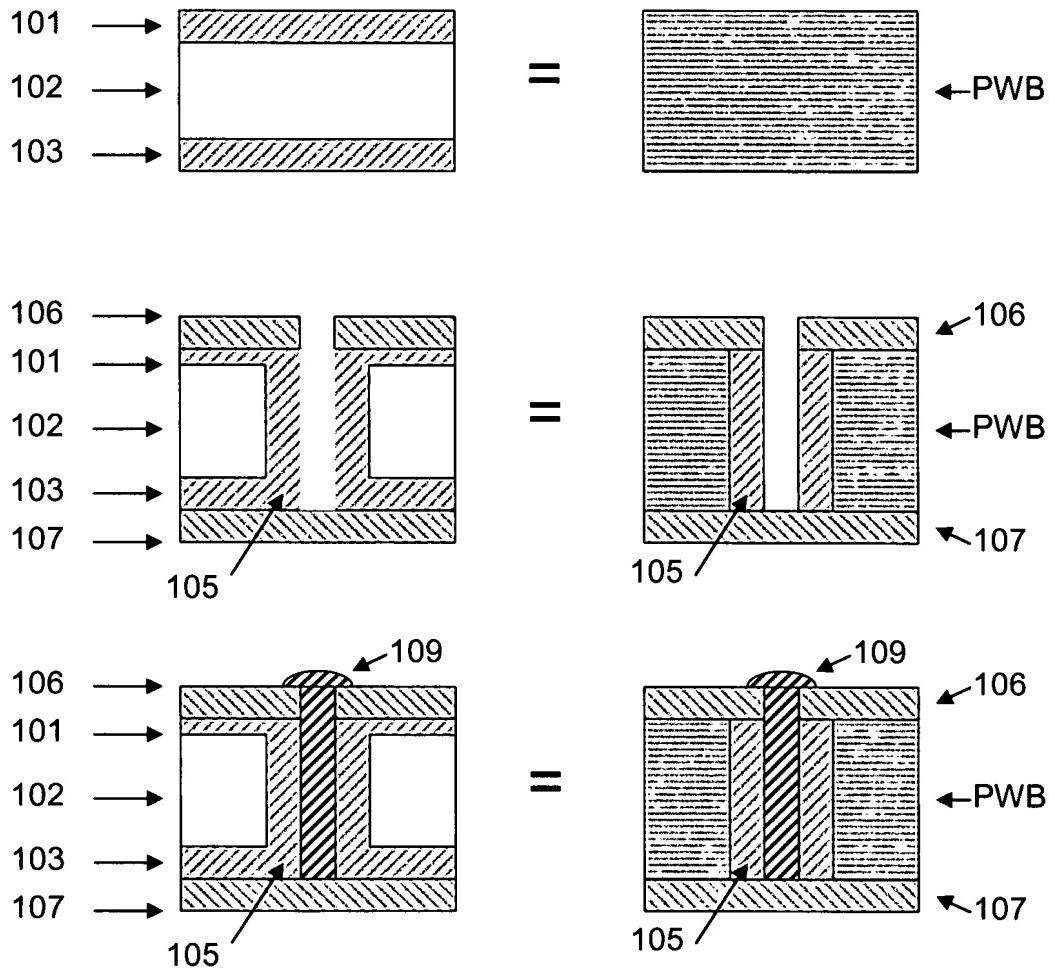
Claims 1-9 remain in the application. Claims 1, 2 and 9 have been amended. Claims 10-32 have been withdrawn.

Claims 1-9 have been rejected under 35 U.S.C. § 112 for informalities. As best understood, the rejection is twofold. First, the Office Action finds some degree of confusion in the repeated use of “conductor” in claim 1. Second, the Office Action finds some degree of confusion as to what surfaces are preventing contact with the copper that fills the hole.

As to the former, claims 1, 2 and 9 have been amended to differentiate between a “first” conductor and a “second” conductor. Applicants note that the use of “first” and “second” is a convenience for identification purposes only to distinguish between repeated instances of “conductor.” It does not imply any numerical, serial or sequential limitation or imply any differences or similarities in characteristics of the various conductors. See *3M Innovative Props. Co. v. Avery Dennison Corp*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). Conductor 105 in the specification is thus a non-limiting example of the claimed “first conductor,” while conductor 109 in the specification would be a non-limiting example of the claimed “second conductor.”

As to the latter, Applicants traverse the rejection. The Office Action appears to be mistaken as to the nature of the printed wiring board, equating it with disclosed dielectric layer 102 (which the Office Action calls “board 102”). However, dielectric layer 102 is but one layer of the printed wiring board of the disclosed embodiment, which includes a first copper layer 101, a dielectric layer 102, and a second copper layer 103. See, e.g., application at page 8, lines 4-8. The

relationship between the printed wiring board and the other layers as disclosed in the non limiting examples of the specification may be shown graphically as follows:



The above¹ clearly shows that photoresist layers 106 and 107, as applied to top and bottom of the printed wiring board, will protect the printed wiring board when the hole is later filled with conductor 109. The above non-limiting teachings thus provide full support for the photoresist

¹ The top two figures are formal representations of Figs. 1A and 1D. The bottom figure corresponds to Fig. 1F, with a potential "nodule" of conductor 109 shown to illustrate how the photoresist protects the PWB from the nodule.

PATENT APPLICATION
Attorney Docket No. 12492.0274

material substantially preventing the second conductor from contacting the first and second sides of the board during said filling.

Accordingly, claims 1-9 are fully supported by the non-limiting examples of the specification. Withdrawal of the rejection and allowance of the same are therefore requested.

The specification has been objected to for lack of specific reference to the individual drawings. The specification has been amended herein to add a basic description. Withdrawal of the objection and allowance of the same are therefore respectfully requested.

As there are no pending art rejections, the application is believed to be in condition for allowance, and a notice to that effect is earnestly solicited.

The Commissioner is hereby authorized to charge any missing or insufficient fee(s) or credit any overpayment, to Deposit Account No. 19-4293 (Case No. 12492.0274).

Respectfully submitted,



Scott D. Watkins
Registration No. 36,715
Steptoe & Johnson, LLP
1330 Connecticut Avenue, N.W.
Washington, DC 20036
Tel: (202) 429-8056
Fax: (202) 429-3902

Date: October 30, 2007